New Memory Technology Migration from Lab to Fab

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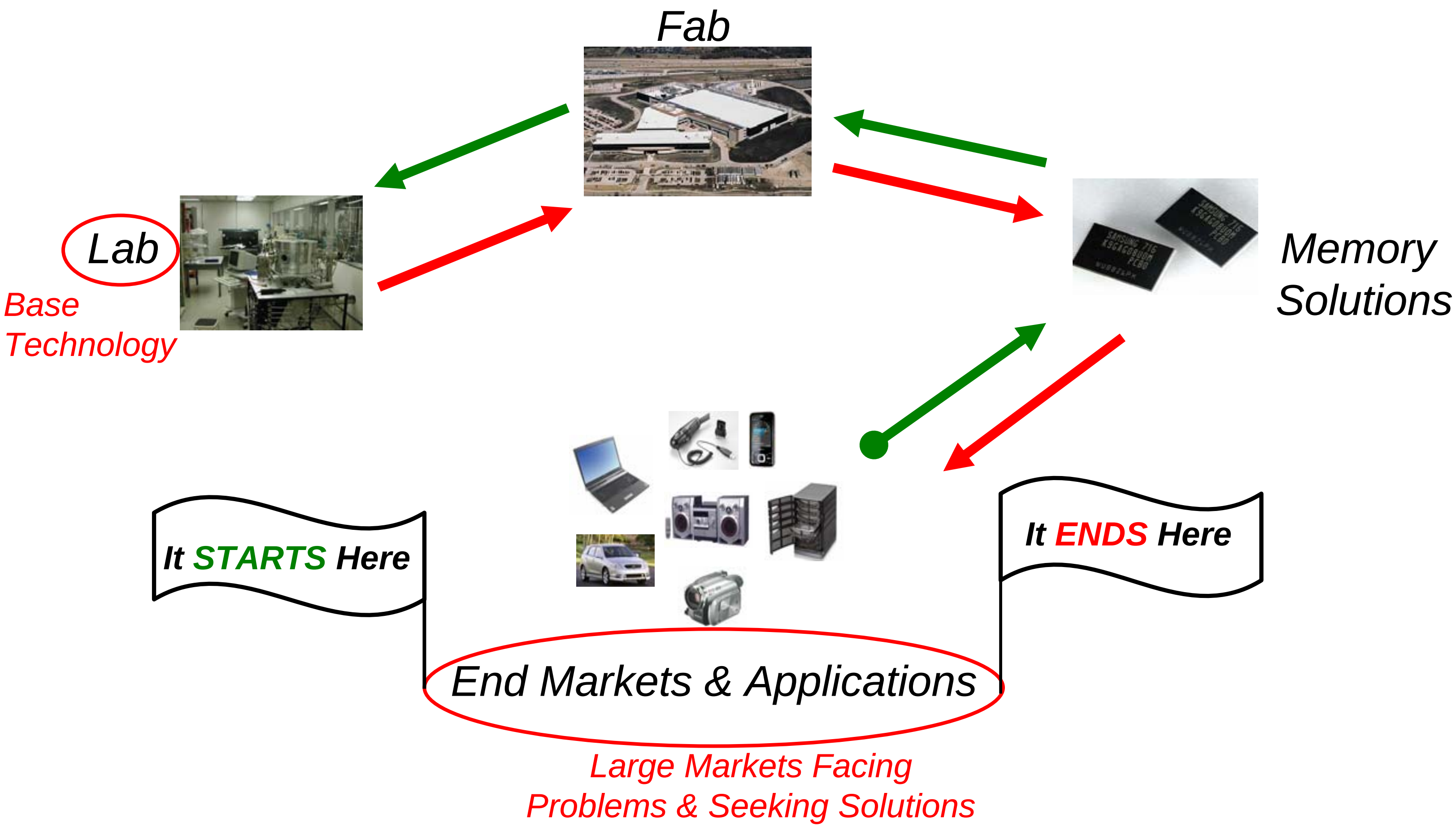
Memory Technology Migration From Lab to Fab

- **For a successful migration, where is the beginning and where is the end?**



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Underpinning of Migration from Lab to Fab

- **The base technology has to solve a problem in order to start the migration**

- **3 Key Questions:**
  - What is the size of the problem ? How bad is the pain ?
  - How well does the base technology address the problems ?
  - How much does it cost to take the base technology from the Lab to the Fab?
    - Does the ROI make sense?

- **Constraints**
  - Existing market expectations have to be respected
    - Fundamentals
    - Power / Performance / Cost
    - Reliability
    - End Use Models

Where is the Market Pull ?

- **Market / End Applications for semiconductor memory:**
  - Consumer, Communication, Computing, Automotive Electronics Industry
- **3 Key Problems:**
  - Cost / Scaling
  - Performance / Power
  - Functional Integration
- **Economic Size of The Problem (just for NVM):**
  - Discrete NVM Market (2011): ~$50B
  - Embedded NVM Market (2011): ~$7B
- **Base Technologies Coming to Rescue:**
  - Evolution of Existing Technologies
    - nanoFG, U-FG, etc.
  - Emerging Memory Technologies
    - RRAM (PCM, PMC, CMO, etc)
    - MRAM, FRAM
    - NEMS, MEMS, etc

Who Will Win?

- **OK, now we have a significant end market facing serious problems and involving billions of dollars of economic value.**

- **Looking at the base technologies in the Lab, can you tell who has the best chance of addressing the problems and winning?**

- **It's all about MARGINS and CONSTRAINTS.**
  - How well does the base technology solve the different problems?
  - How does this technology impact all the CONSTRAINTS?
  - Example:

		Existing Technology	**Technology X**			
	Metric	**Production**	**Lab**	**Fab**	**Qualifciation**	**Production**
	Fundamentals	OK	OK			
Higher is Better →	Performance	1 X	100 X			
Lower is Better →	Power	1 X	1 X			
Lower is Better →	Cost	1 X	1 X			
Higher is Better →	Reliability	1 X	1 X			
	End Use Model	OK	OK			

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Candidate Technologies

			Emerging Technology Options for Non-Volatile Memory		
		Existing Non Volatile Memory Solutions	Phase Change Ovonics	MRAM	PMC Technology (Arizona State Univ.)
	Fundamentals	OK	OK	OK (?)	OK
Higher is Better →	WRITE Performance	1	100 X	1000 X	500 X
Higher is Better →	READ Performance	1	10 X	10 X	50 X
Lower is Better →	WRITE Power	1	1 X	1 X	0.001 X
Lower is Better →	READ Power	1	0.1 X	0.1 X	0.01 X
Lower is Better →	Cost	1	0.5 X	2 X	0.1 X
Higher is Better →	Reliability	1	??	??	??
	End Use Model	OK	OK	OK	OK

Always Bet on the Technology with the Largest MARGINS

Requirement to Win: Withstand Trauma of Migration

- **Base technology must exhibit orders of magnitude improvements and margins in key CONSTRAINTS to withstand the qualification and commercialization process**

- **Lab to Fab is 12 rounds of vicious punishment**